Multiprocessor Scheduling taking into account Energy Harvesting and Storage

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Outline

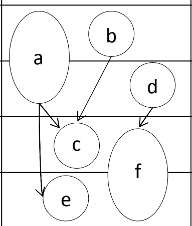
- Introduction
- Problem Formulation
- Experimental result
- Conclusion

Time-Constrained Scheduling

- Traditionally, we minimize hardware cost (processor and memory) and energy cost (power consumption rate) assuming a fixed-capacity power supply
- In an environment that relies on harvested energy, the task scheduler should take into account both energy generation, storage and retrieval .

Motivational Example(1/3)

- Scheduling Without Battery

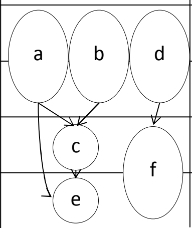


Step	Schedule	Energy Consumed	Generator Output	Battery			
				Discharge	Charge	Storage	
						Before	After
1		5	5	0	0	0	0
2		5	5	0	0	0	0
3		5	5	0	0	0	0
4		5	5	0	0	0	0
Hardware: Core = 2 Generator = 5 Battery = 0							

Motivational Example(2/3)

- Scheduling With Battery

Step	Schedule	Energy Consumed	Generator Output	Battery: Discharge	Battery: Charge	Storage: Before	Storage: After
1		3	4	0	1	0	1
2		3	4	0	1	1	2
3		5	4	1	0	2	1
4		5	4	1	0	1	0
Hardware: Core = 3 Generator = 4 Battery = 2							



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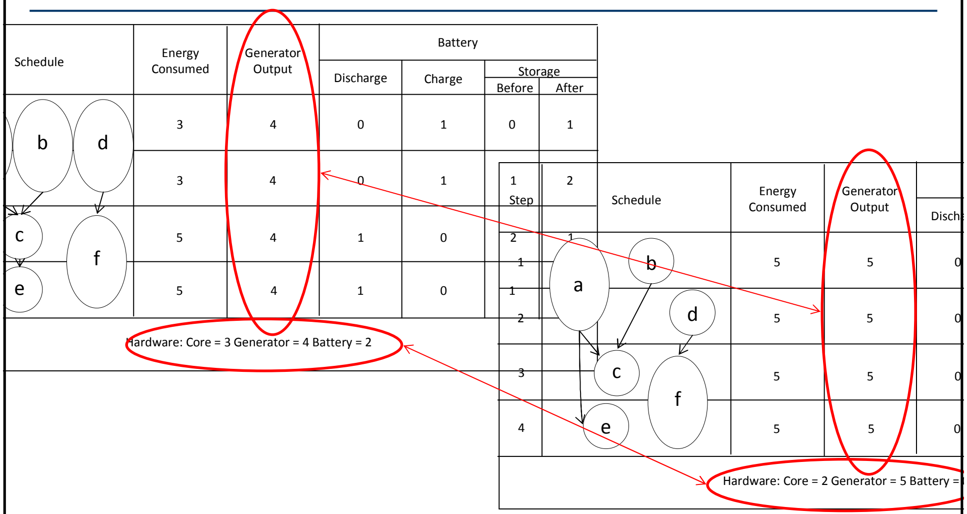
Motivational Example(3/3)



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Problem Definition

- Input
  - A task graph
  - Performance target (the time-constraint to complete the task)
  - Unit costs of generator, battery and hardware DVFS cores.
  - A library of DVFS cores
- Output
  - A scheduled task graph meeting the time-constraint.
  - A scheduled time and speed mode of each task
  - Number of cores (maximum parallelism over all time)
  - Generator capacity (maximum energy generated over all time)
  - Battery capacity (maximum energy stored over all time)

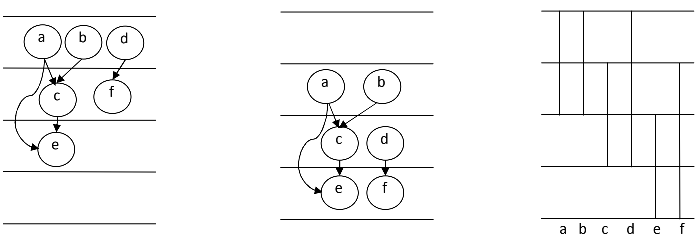
Assumptions

- Homogeneous multicores
- Negligible communication and power-switching overhead
- Four modes for DVFS cores
- SECS SuperESCalar Simulator
- Applications composed of image compression, encryption and channel coding tasks

Algorithm

- Time-constrained Total-Hardware-Cost-minimized scheduling
  - As Soon As Possible (ASAP)
  - As Late As Possible (ALAP)
  - Integer Linear Programming (ILP)

ASAP & ALAP



ASAP (S_i)   ALAP (L_i)   Mobility

Integer Linear Programming (1/6)

- CPLEX ILOG (ILP Tool): mixed integer linear programming [16]
- Parameters
  - *Cc, Cg* and *Cb* denote unit cost of core, generator, and battery, respectively.

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Integer Linear Programming (2/6)

- Variable
  - *Num_cores* : an integer variable denoting the number of cores needed
  - *Generator* : an integer variable denoting the maximum output power per clock cycle of the generator
  - *Battery* : an integer variable denoting the storage capacity of the battery
  - $X_{i,j,k}$ are 0-1 integer variables associated with task T_i. $X_{i,j,k}$ = 1 if T_i is scheduled into step j and operated k clock cycles (k = 1 or 2); otherwise, $X_{i,j,k}$ =0

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Integer Linear Programming (3/6)

Task	T_a	T_b	T_c	T_d	T_e	T_f
ILP Variable one cycle						
Step 1	$X_{a,1,1}$	$X_{b,1,1}$		$X_{d,1,1}$		
Step 2	$X_{a,2,1}$	$X_{b,2,1}$	$X_{c,2,1}$	$X_{d,2,1}$		$X_{f,2,1}$
Step 3			$X_{c,3,1}$	$X_{d,3,1}$	$X_{e,3,1}$	$X_{f,3,1}$
Step 4					$X_{e,4,1}$	$X_{f,4,1}$
ILP Variable two cycles						
Step 1	$X_{a,1,2}$	$X_{b,1,2}$		$X_{d,1,2}$		
Step 2			$X_{c,2,2}$	$X_{d,2,2}$		$X_{f,2,2}$
Step 3					$X_{e,3,2}$	$X_{f,3,2}$
Step 4						

Integer Linear Programming (4/6)

- Minimizing
  - *Cc * Num_cores + Cg * Generator + Cb * Battery*
- Subject to
  - Power consumption
    - No more than B_{i-1} + Generator

      (Bi means energy stored in the battery prior Step i)

      $$\sum_{T_i \in I} [(4 * \mathrm{X}_{i,j,1} + 1 * \mathrm{X}_{i,j,2}) + B_i - (B_{i-1} + Generator)] \le 0$$
    - Battery capacity $\sum_{T_i \in I} (B_i - Battery) \le 0$
    - Capacity limit w/r to generator $Battery - 2 * Generator \le 0$

Integer Linear Programming (5/6)

– Mutually excusive $\sum_{j=Si}^{Li} X_{i,j,1} + \sum_{j=Si}^{Li-1} X_{i,j,2} = 1 \quad for\ 1 \le i \le n$

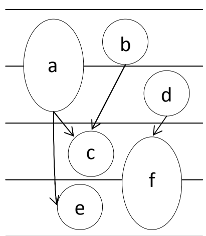
– Total hardware $\sum_{T_i \in t} (X_{i,j,1} + X_{i,j,2})$ - $Num\_cores \le 0$

– Dependency $X_{i,j,1} + X_{m.n.k} \le 1$ for $S_i \le j \le L_i,\ S_i \le n \le j, 1 \le k \le 2$

$X_{i,j,2} + X_{m,n,k} \le 1$ for $S_i \le j \le L_i,\ S_i \le n \le (j+1), 1 \le k \le 2$

for all $T_i \rightarrow T_m$

Integer Linear Programming (6/6)



$X_{a,1,2}, X_{b,1,1}, X_{c,3,1}, X_{d,2,1}, X_{e,4,1}, X_{f,3,2} = 1$

- Cc = 2, Cg = 1, Cb = 0.001
- Num_cores = 2, Generator = 5, Battery = 0

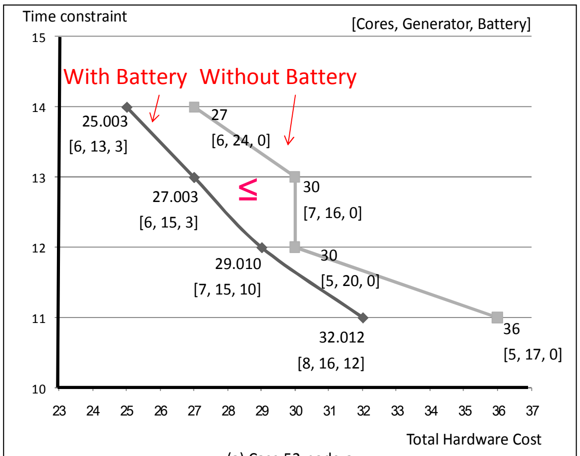
Experiment Setting

- Cost model of generator [20]
  - a 12V and 5W panel costs USD 35.00.
- Cost model of battery [21]
  - NiCd AA Cell 0.6Ah x7.5V x0.0075$/Wh =0.03375$

NiCd AA Cell	Capacity (mAh)	Voltage	Cost per KWh	Energy per cycle(Wh)
	600	7.5	7.5	0.6*7.5 = 4.5

- Cost function of minimization
  - 2 x Num_cores + generator + 0.001 x battery.

Design Space (Artificial Case)

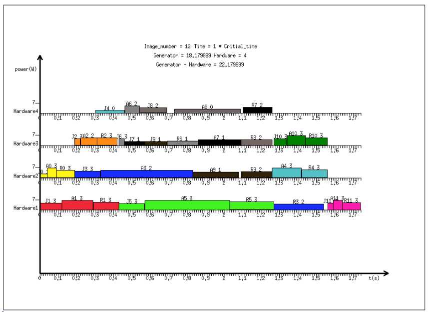
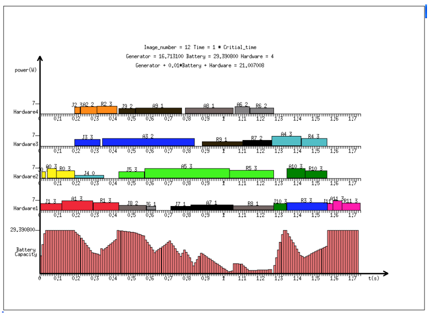


(a) Case 52-node-a

DVFS Parameters Based on SECS Simulation Results

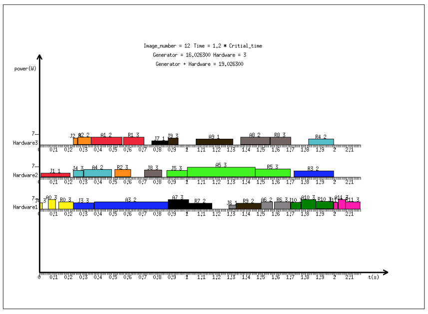
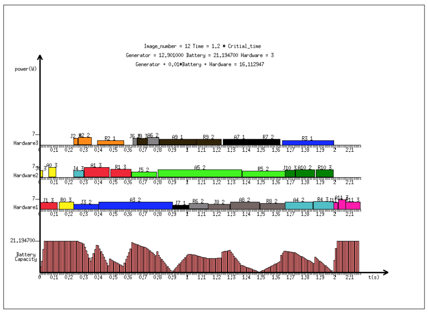
	Type	Size	Voltage/Frequency	Power(W)	Time(s)
Image12.bmp 640*480 900KB	JPEG Source Coding	97.7KB	0.8V/0.711GHz	1.95819	0.32
			0.9V/1.007 GHz	2.64207	0.23
			1.0V/1.313 GHz	3.47367	0.17
			1.1V/1.600 GHz	4.50778	0.14
	AES Encryption	97.7KB	0.8V/0.711 GHz	2.87483	1.05
			0.9V/1.007 GHz	3.90190	0.74
			1.0V/1.313 GHz	5.14090	0.57
			1.1V/1.600 GHz	6.67996	0.46
	RS Channel Coding	130KB	0.8V/0.711 GHz	2.35421	0.53
			0.9V/1.007 GHz	3.20254	0.38
			1.0V/1.313 GHz	4.23445	0.29
			1.1V/1.600 GHz	5.51935	0.23

Usage of Battery → Lower Total Cost (1/4) [1.0X TC]

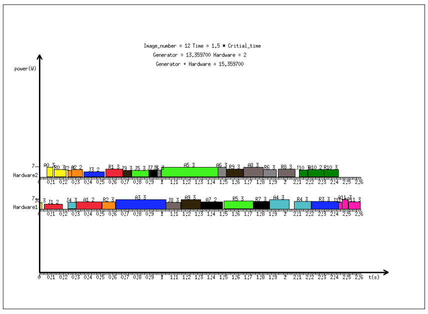
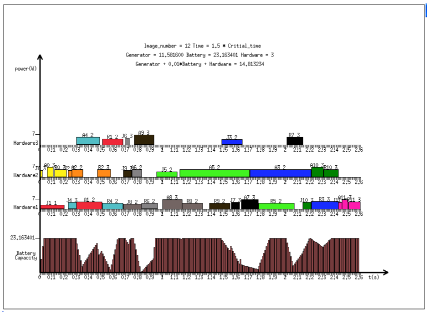
4	Processor	4
18.1799	Generator	16.7131
0	Battery	29.39
22.1799	Total	21.1287

Usage of Battery → Lower Total Cost (2/4) [1.2X TC]

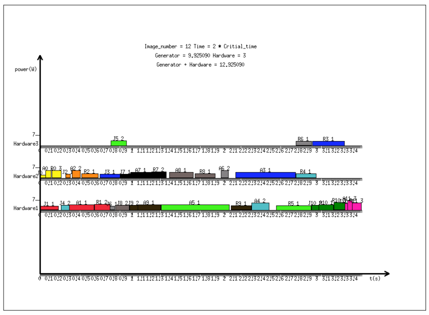
3	Processor	3
16.0263	Generator	12.901
0	Battery	21.19
19.0263	Total	17.8041

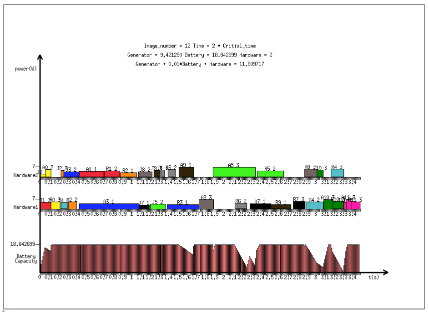
Usage of Battery → Lower Total Cost (3/4) [1.5X TC]

2	Processor	3
13.3597	Generator	11.5816
0	Battery	23.16
15.3597	Total	14.9539

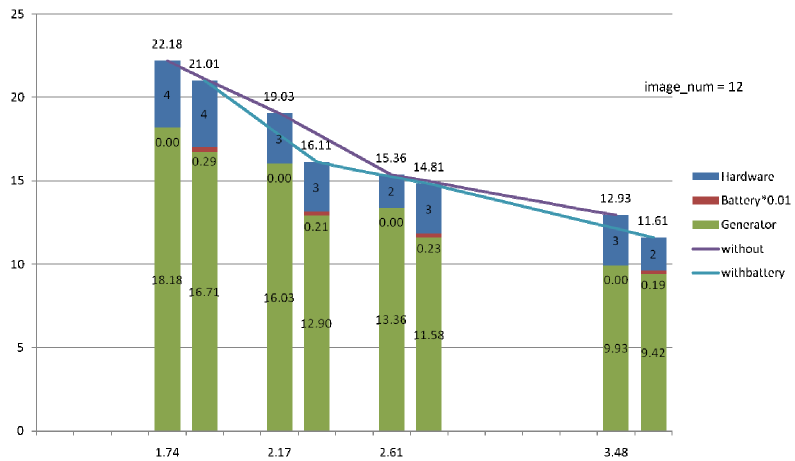
Usage of Battery → Lower Total Cost (4/4) [2.0X TC]





3	Processor	2
9.92509	Generator	9.42129
0	Battery	18.84
12.92509	Total	11.60969

Total Cost vs Time Constraints and Battery Usage



Conclusion

- A time-constrained scheduler minimizing total hardware cost including
  - Processor Cores
  - Energy Harvester
  - Energy Storage
- Trade-Off among three types of resources
- Evaluation with data (source coding, cryptography, channel coding) from SESC simulator